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10/581,849	10/16/2007	Gunther Leising	U 016328-0	4589

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LADAS & PARRY LLP
26 WEST 61ST STREET
NEW YORK, NY 10023

EXAMINER	
TAVLYKAEV, ROBERT FUATOVICH	

ART UNIT	PAPER NUMBER
2883	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/581,849	LEISING ET AL.	
	Examiner	Art Unit	
	ROBERT TAVLYKAEV	2883	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 16, 21 – 23, 26 – 28, 30, 32, 34 and 38 – 49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 16, 21 – 23, 26 – 28, 30, 32, 34 and 38 – 49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's amendment filed 10/29/08 is acknowledged. Claims 1 - 16, 21 – 23, 26 – 28, 30, 32, and 34 have been amended, and claims 38 – 49 added. Claims 1 - 16, 21 – 23, 26 – 28, 30, 32, 34 and 38 – 49 are pending.

Response to Arguments

2. The Rejection of claims 1 - 16, 21 – 23, 26 – 28, 30, 32, and 34 under 35 USC § 112, second paragraph, has been withdrawn due to the Applicant's amendments. The Applicant's arguments filed 10/29/08 regarding rejections under 35 USC § 102(e) and 103(a) have been fully considered but they are not persuasive. Furthermore, the arguments are moot in view of the new grounds of rejections, as necessitated by the Applicant's amendments.

The Applicant alleges that the teaching of Iwaki always refers to a three-layer structure with a lower cladding layer, a waveguide core layer, and an upper cladding layer, as opposed to the Applicant's disclosure, wherein a single layer structure is detailed.

The Examiner respectfully disagrees. The Applicant appears to have been confused by a difference existing between the standard waveguide nomenclature/ terminology used by Iwaki and that used throughout the specification. A simple visual comparison of Fig. 1 of Iwaki with Fig. 1 of the present application immediately shows that the elements disclosed by Iwaki and the present application both have a waveguide core layer ((105) and (6) respectively) surrounded by a cladding layer ((106) and (3) respectively, each core and cladding layer being part of a corresponding optical layer. The cladding layer disclosed by Iwaki is unchanged by irradiation,

while the optical core layer is structured by irradiation. Overall, the cladding layer shown in Fig. 1 of Iwaki is substantially equal to the optical layer described by the Applicant's specification.

Claim Objections

3. Claims 32, 45, and 46 are objected to because of the following informalities. The claims are shown as depending on claims 31 and 29, however, claims 31 and 29 have been cancelled. For the purposes of this Action, the dependences are interpreted as follows: claim 32 depends on 30, claim 45 on 28, and claim 46 on 45. Appropriate corrections are required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-7, 10-15, 21-23, 26, 27, 39 – 43, and 47 - 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwaki et al (US Pub. No. 2004/0001661 A1) in view of "Two-photon polymerization initiators for three-dimensional optical data storage and microfabrication," by Cumpston et al, Nature, vol. 398, March 1999, pp. 51 – 54 (hereinafter Cumpston).

Regarding claim 1, Figs. 1 and 15 of Iwaki disclose a printed circuit board element including at least one optical waveguide (105) provided in an optical layer (106/104) and at least one optoelectronic component (103) in optical connection with the optical waveguide (105), characterized in that the optoelectronic component (103) is embedded in the optical layer (106), that the optical waveguide (105) adjoins the optoelectronic component (103), and that the optical waveguide is structured by irradiation (par. [0048] and [0054]) within the optical layer (106), the latter being a single layer of a photorefractive material. Iwaki cites (par. [0054]) that the photorefractive material is capable of photon absorption processing, but does not detail as to whether a single-photon or a multi-photon process (both processes being well known in the art)

is used. In this regard, Cumpston describes (e.g., Fig. 3c; page 3, 3rd full paragraph) a two-photon absorption process for direct writing of optical waveguides (e.g., in polymer materials). Therefore, it would have been obvious to a person of ordinary skill in the art that the waveguide disclosed by Iwaki may be structured by a two-photon absorption process if the optical layer has a proper material capable of such processing, as described by Cumpston. A key advantage of two-photon absorption processing is its quadratic dependence on optical power, which can tightly confine a writing area and hence provide a high spatial resolution in three dimensions when writing is done using a tightly focused optical beam (Abstract of Cumpston).

Regarding claim 2, Fig. 6 and 1 of Iwaki show that the optoelectronic component (103) with one side may border upon a substrate (129b) carrying the optical layer (106), or a cladding layer (106) applied thereon, respectively. It is obvious that the board element in Fig. 1 may have a substrate disposed similarly to the substrate (129b) in Fig. 6 in order to increase the mechanical stability/rigidity of the board element (par. [0059] of Iwaki).

Regarding claim 3, the optoelectronic component (103) in Fig. 1 of Iwaki is embedded in the optical layer (106) on all sides.

Regarding claim 4, the optical layer (106) in Fig. 1 of Iwaki may be realized as a flexible layer, such as a polymer layer (see paragraph [0053]).

Regarding claim 5, Fig. 1 shows two optoelectronic components ((103) and (101)), connected with each other via the optical waveguide (105), that are embedded in the optical layer (106).

Regarding claims 6 and 7, the optoelectronic component (103) in Fig. 2 of Iwaki borders upon a heat-dissipation layer (121c) connected to a heat-sink part (125). The heat-dissipation layer (121c) is formed by a patterned inner ply (see Fig. 7B).

Regarding claims 10-12, the optoelectronic component (103) in Fig. 6 of Iwaki borders on an electrically conductive distribution layer (to the left from the part 121a), the latter being connected with an external contact (141) through a via (140) provided in a substrate (129a) that carries the optical layer (104) and the distribution layer.

Regarding claims 13 and 14, Fig. 6 of Iwaki shows a printed circuit board layer ((129a) or (129b)) having a patterned, conductive inner ply (comprising the part (121a)) and/or outer ply (comprising the part (141) or the 2 electrically conductive parts on the bottom surface on the layer (129b)) is applied on at least one side of an electrically insulating optical layer (104). Furthermore, the optoelectronic component (103) is contacted through vias (part (140) and the next one to the right) provided in the printed circuit layer (129a). Fig. 2 of Iwaki shows a contact to the optoelectronic component (103) made through a via (125) in the optical layer (104).

Regarding claim 15, Fig. 8 of Iwaki shows an electronic component (113) connected with the optoelectronic component (103). Iwaki further teaches (see paragraph [0085]) that there may be a printed circuit board layer placed between the electronic component (113) and the optical layer (106). Fig.6 explicitly shows at least one such printed circuit board layer (parts (129a) and (129b)), to which the electronic component (113) would be mounted to.

Regarding claim 21, Figs. 7A – 7I of Iwaki show steps of a method for producing a printed circuit board element, for example, one shown in Fig. 2, that has all the limitations of claim 1 (see argument for claim 1 above) and some additional features. Furthermore, the

disclosed method has all of the steps of claim 21 as well as additional steps. In particular, the disclosed method produces a printed circuit board element having recesses to be filled with a light transmitting resin (109) (par. [0055]). Iwaki et al do not explicitly illustrate a method for producing a printed circuit board element without recesses, such as that shown in Fig. 1. However, it would have been obvious to a person of ordinary skill in the art that the printed circuit board element shown in Fig.1 can be produced using the following sequence: (a) the step shown in Fig. 7D, which illustrates a step of mounting at least one optoelectronic component, e.g., (103) to a substrate (119); (b) the step shown in Fig. 7B, which illustrates a step of applying an optical layer (106) to the substrate (119), the optical layer being comprised of an optical material changing its refractive index upon photon irradiation. Without the recesses shown in Fig. 7b and the optoelectronic component (103) already mounted to a substrate (119), the optical layer (106) would embed the optoelectronic component (103); (c) the step shown in Fig. 7A, which illustrates a step of producing, by photon irradiation, a waveguide structure (105) in the optical layer (106), the waveguide structure being surrounded by the remaining optical layer (106), in order to adjoin the optoelectronic component (103). The motivation for using a method with such step sequence is that it is a simplest and shortest sequence that can be used to produce the printed circuit board element shown in Fig. 1 of Iwaki et al. Therefore, production cost can be reduced, since the additional steps, which are shown in Figs. 7A – 7I and needed for the more complicated printed circuit board element shown in Fig. 2, would be superfluous for the printed circuit board element shown in Fig. 1.

Regarding claim 22, Fig. 1 of Iwaki shows two optoelectronic components (i.e., parts (101) and (103)), which are embedded in the optical layer (106) and thereafter are connected

with each another by the optical waveguide (105) directly adjoining the same. It would have been obvious to a person of ordinary skill in the art that the board element in Fig. 1 may have a substrate, which is used for mounting the two optoelectronic components and disposed similarly to the substrate (129a) in Fig. 6, in order to increase the mechanical stability / rigidity of the board element (see paragraph [0059] of Iwaki).

Regarding claim 23, Fig. 7B of Iwaki shows that after the production of the optical waveguide structure (105) in the optical layer (106), a printed circuit board layer (119) including a conductive inner ply (comprising the parts (121a) and (121c)) is applied to at least one side of the optical layer (106).

Regarding claims 42 and 43, Figs. 6 and 7B of Iwaki show that the inner ply (comprising the parts (121a) and (121c)) may be patterned before applying the printed circuit board layer ((119) or (129a)) to the optical layer (104). Figs. 6 and 7H - 7I show that the outer ply (comprising (121b) or (141)) can be patterned after such application.

Regarding claim 26, Fig. 6 of Iwaki shows that vias (comprising (140) and (125)) are provided in the optical layer (104) and in the printed circuit board layer (129a), in coordination with the respective optoelectronic component (103), and that electrically conductive connections to the optoelectronic component can be established through the vias.

Regarding claim 27, Fig. 8 of Iwaki shows that the optoelectronic component (103) is conductively connected with an associated electronic component, i.e. a driving part (113). Fig. 8 does not explicitly show a printed circuit layer or a substrate. However, it would have been obvious to a person of ordinary skill in the art that there may be a printed circuit layer (which is included between the part (113) and the optical layer (106) and is used for mounting the part

(113)), because Iwaki illustrates such a printed circuit layer in Fig. 6 and teach that this arrangement is desirable as providing increased mechanical stability/rigidity of the entire printed circuit board element (par. [0059] of Iwaki).

Regarding claims 40 and 48, Fig. 15 of Iwaki discloses an optical waveguide (105) provided with a lens structure (109) on its end adjacent an optoelectronic component (101), the latter being a light reception device. The lens structure at least partially encloses the optoelectronic component (101) and is used for focusing light into the optoelectronic component (101). The focusing property depends on the refractive index of the material used to form the lens structure (109). Iwaki does not explicitly state that the lens structure (109) can be made a part of the optical waveguide (105). However, Iwaki does cite (see paragraph [0098]) that the refractive index of the material should be higher than that of the optical layer (104). Thus, it would have been obvious to a person of ordinary skill in the art that the material of the optical waveguide (105) can be used to form the lens structure (109) and be integral with it, since the refractive index of optical waveguide (105) satisfies the above condition. The motivation for forming the lens structure (109) as a part of the optical waveguide (105) is that such a structure would have a reduced the number of needed materials, can be produced in a single step, and reduces cost, while still providing the benefit of an improved light collection efficiency.

Regarding claims 39, 41, 47, and 49, Fig. 3c of Cumpston shows a tapered optical waveguide that is widened in a funnel-shaped manner. It is noted that tapered waveguides are well known in the art to be used for coupling to optoelectronic components, such as semiconductor lasers. Cumpston further states (page 53, 3rd full paragraph) that the produced waveguide structures can be photonic bandgap structures, which are also known as photonic

crystal structures. The latter are well known in the art as being capable of providing light confinement and mode shaping via a variety of topologies (lenses, tapers, etc.)

7. Claims 8, 9, 28, 30, 32, 38, and 44 – 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwaki et al (US Pub. No. 2004/0001661 A1) in view of "Two-photon polymerization initiators for three-dimensional optical data storage and microfabrication," by Cumpston et al, Nature, vol. 398, March 1999, pp. 51 – 54, as applied to claims 1 and 21 above, in view of Yoshimura et al (US Patent No. 6,684,007 B2).

In regard to claims 8, 9 and 28, Fig. 8 of Iwaki shows that the optoelectronic component (103) is used with an associated electronic component, i.e. a driving component (113). In Fig. 8, the driving component (113) is shown to be positioned on one side of the board. However, Iwaki's invention also includes an embodiment, wherein the driving device (113) is arranged inside the board (par. [0085]), thus making it an embedded unit. The optoelectronic component (103) (e.g., a light emission device (see paragraph [0046])), if combined with the driving component (113) (i.e. an electronic driver), is an optoelectronic chip. Therefore, Iwaki teaches all of the subject matter, except for stating that the optoelectronic component (103) may be combined to form a unit with an associate electronic component (113) (shown in Figs. 6 and 8). Yoshimura et al disclose a printed circuit board element, which may have a polymer optical waveguide, electrical layers, and vias, and teach (see col. 62, lines 28-66) that a VCSEL (optoelectronic device) with an integrated driver (electronic component) or a photodetector (optoelectronic device) with an integrated amplifier (electronic component) may also be used. Thus, it would also have been obvious to a person of ordinary skill in the art that the

optoelectronic component (103), which is embedded in the optical layer (104) and mounted to a substrate, as disclosed by Iwaki, can be combined to form an optoelectronic chip unit with an associate electronic component, as disclosed by Yoshimura et al. The motivation is that a smaller footprint and higher component packing density can be realized by such integration, compared to using individual components.

Regarding claim 44, Iwaki teaches (par. [0085]) that the disclosed printed circuit board element can include multilayer boards on one of both sides of the optical layer. Two or more layers in a multilayer board can represent a cover layer and a substrate with the cover layer being provided before applying the optoelectronic component thereto.

Regarding claim 30, Iwaki further teaches (par. [0065]) that some layers can be made of a light blocking material. Such material would absorb light. It would have been obvious to a person of ordinary skill in the art that if a substrate layer is made of a light blocking material, then a cover layer comprising an optically transparent material and acting as an optical buffer would be required to be applied to the substrate, in order to separate the light-absorbing substrate and the optical layer and avoid high optical loss. The motivation for such a substrate / cover layer combination is that both low-loss optical transmission and reduced optical cross-talk due to suppressed stray light (par. [0065] of Iwaki) can be obtained.

Regarding claims 32, 45, and 46, Fig. 6 of Iwaki shows that electrical connections for the optoelectronic components (103) and (101) are established throughout an electrically conductive distribution layer (comprising parts (121a) and (121c)), the distribution layer being configured as a heat-dissipation layer. Fig. 6 makes it obvious that the distribution layer can be applied to a substrate (129a) and subsequently patterned.

Regarding claim 38, Yoshimura teaches (e.g., col. 62, lines 28 – 66) that the optoelectronic component can be a VCSEL component, while Fig. 15 of Iwaki shows that the optical waveguide (which can comprise (105) and a part of (109) before the front (right) face of (101); see also arguments for claim 40 above) can adjoin the optoelectronic component with an arc-shaped transition.

8. Claims 16 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwaki et al (US Pub. No. 2004/0001661 A1) in view of "Two-photon polymerization initiators for three-dimensional optical data storage and microfabrication," by Cumpston et al, Nature, vol. 398, March 1999, pp. 51 – 54, as applied to claims 1 and 21 above, and as evidenced by Pollak et al (US Pat. # 5,255,070).

Regarding claims 16 and 34, Iwaki teaches all the subject matter, except for explicitly stating that the optoelectronic component (103) can be produced in situ on the substrate by a thin-film technique. It is noted that a great variety of thin-film techniques, such as molecular beam epitaxy (MBE) and chemical vapor deposition (CVD), are well known in the art and would have been obvious to a person of ordinary skill in the art. The motivation for using a thin-film technique is that it allows a simultaneous production of a number of optoelectronic components and can achieve high integration density. Pollak provides (col. 1, lines 14 – 24) evidence that thin-film techniques (MBE and MOCVD) are routinely used for making optoelectronic components (e.g., quantum wells that are the key stone of quantum-well lasers).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

"Three-dimensional microfabrication with two-photon-absorbed photopolymerization," by Maruo et al, optics Letters, vol. 22, No. 2, Jan 1997, pp. 132 134, describes direct writing using a two-photon absorption process.

Hill et al (US Pat. # 5,367,588) disclose a process of changing refrqctive index in waveguides using a two-photon absorption process.

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT TAVLYKAEV whose telephone number is (571)270-5634. The examiner can normally be reached on Mon - Thur 9 am - 6 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank Font can be reached on 571-272-2415. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Robert Tavlykaev/
Patent Examiner, Art Unit 2883

/Frank G Font/
Supervisory Patent Examiner, Art Unit 2883

2/12/09